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Design of BIST with Low Power Test Pattern Generator

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Abstract: Mixed mode BIST schemes use pseudo-random patterns to detect most faults. Theoretical analysis suggests that significantly more care bits can be encoded in the seed of a Linear Feedback Shift Register (LFSR). In this paper we implement low power BIST for 32-bit Vedic multiplier. Main aspect of this is to implement low power BIST with increased fault coverage. This use the LFSR as test pattern generator with changing the seed values for every 2 power m cycle, so for this purpose which uses the counter for monitoring the number of cycles. The objective of this work is to reduce power dissipation in BIST with increased fault coverage. Various methods of pattern generation are compared keeping in view of power consumption. For this purpose m bit binary counter & gray code generator is used. Signature analysis is done with the help of Multiple input Signature Register (MISR). The signature of MISR will indicate whether the circuit under test (CUT) i.e Vedic multiplier is faulty or not. The results are tabulated and compared. From the implementation results, Simulation is carried out in Xilinx ISE and the design is implemented using Vertex 5 Field Programmable Gate Array (FPGA).

Keywords: Vedic multiplier, Test Pattern Generation, MISR, CUT.

I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly. These applications require low power dissipation. The main aim of these devices is to reduce the power dissipation with high fault coverage. Generally power dissipation of a system in test mode is more than in normal mode. Testing of integrated circuits is important to ensure high level of quality in products. The Built-In-Self-Test (BIST) is one of most popular test solutions to test the embedded cores. Test pattern generation is vital in any BIST circuit. Since off-chip communication between the FPGA and a processor is bound to be slower than on chip communication and in order to minimize the time required for adjustment of the parameters, the built in self test approach is proposed for this method.

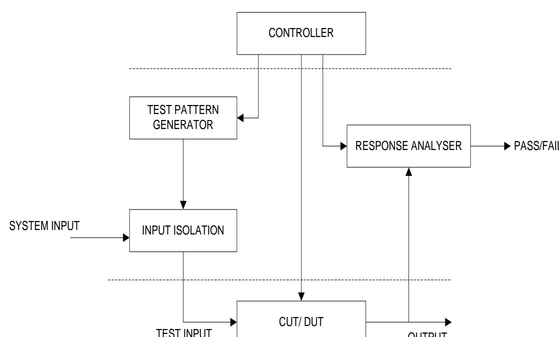

Fig. 1 Block diagram of Built In Self Test

The generic BIST is shown in Fig. 1. BIST solution consists of several blocks given below. a) Circuit under test (CUT) : It is the portion of the circuit tested in BIST mode. It can be combinational, sequential or a memory. b) Test pattern Generator (TPG): This is a circuit to be tested, a way to compress those results & way to analyze them. It generates the test patterns for CUT. Here a Linear feedback shift register is used to generate patterns. Patterns are generated in pseudo random fashion. c) Test controller: It controls the test execution. It provides the control signal to activate all blocks. If control signal is 0, then BIST is said to be in test mode & if 1, normal mode. d) Response Analyzer: It acts as a comparator with stored responses. Compares the test output with the stored response and shows whether the chip passes or fails the test.

BIST architecture is based on Linear feedback shift register whose input bit is logic function of its previous state. An LFSR basically consists of an interconnection of D-flip-flops, XOR gates, forming a shift register with feedback. Mainly LFSR"s are used for pseudo random generation such as TPG"s, ATPG, code convolution techniques.

The initial value of LFSR is called seed value. This seed value is always represented in Galois field format or normal binary format also called characteristic polynomial expression of a unit. The initial value of LFSR should be non zero value i.e any one of the bit should be high. If it is zero value then LFSR will be in zero lock state where it produces only zero value to all the clock pulses.

The selection of characteristic polynomial is based on the number of faults to be covered.

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Before the overall design is synthesized, the four LFSR based test pattern generations is incorporated into CUT.

There are different test pattern generators. They are
A. LFSR Type I
B. LFSR Type II
C. Multiple polynomial
D. Cellular Automaton LFSR

All these circuits are described in Verilog HDL and implemented on Vertex 5 FPGA.

A.LFSR Type I:
LFSR type I is commonly used TPG and is called External LFSR. It consists of D flip flops and XOR gates. The XOR gates are in external feedback. LFSR can cycle through 2^{n-1} distinct states, all zero state is omitted. LFSR type I is

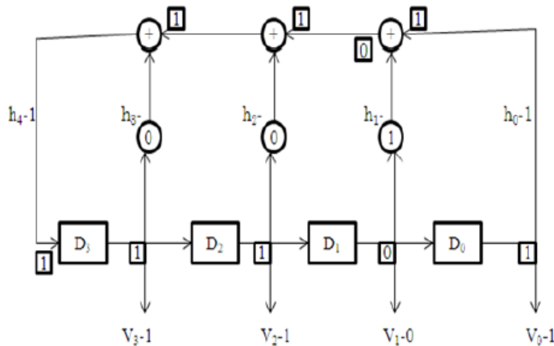

Fig 2: LFSR Type 1

B.LFSR Type II:
LFSR type II is called Internal LFSR. It has the linear elements interspersed between flip flops. There are n flip-flops, so it is called an n-stage LFSR. LFSR can cycle through 2^{n-1} distinct states, all zero state is omitted. The main difference between LFSR type I & type II is that in type I the XOR gates are in external feedback and in type II the XOR gates are internal i.e. in between the flip-flops.

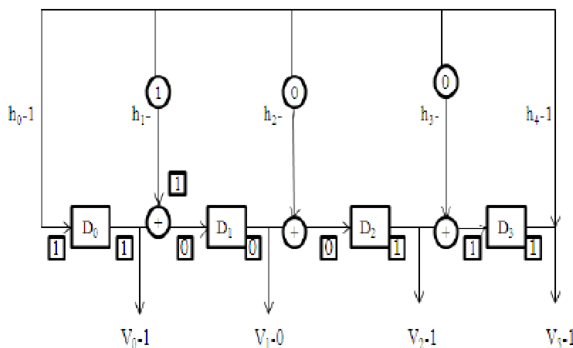

FIG 3: LFSR Type 2

C. Multiple polynomial:
Multiple polynomial LFSR can change characteristic polynomial in determined time. Here a decoding logic is present and its input bits are given to three AND gates. Using this different seed values are generated. This decoding logic is used to select the particular pattern in a row of patterns. Circuit for Multiple polynomial is shown in Fig 4.

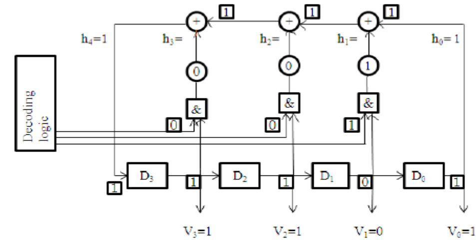

FIG 4: Multiple polynomial

D. Cellular Automaton LFSR:
Cellular Automaton (CA) consists of cells. Each cell is build from memory element (Flip-flop) and combinational element. Input to the combinational part of cell is driven from neighbouring cells and the cell itself. It will generate all 2n-1 patterns for an n cell CA. The all zero pattern is not generated by the CA, just like an LFSR, without adding additional hardware. CA is used in the pattern generator and response analyser. LFSRs are more popular because of their compact and simple design. Cellular Automaton LFSR are more complex to design but provide patterns with higher randomness

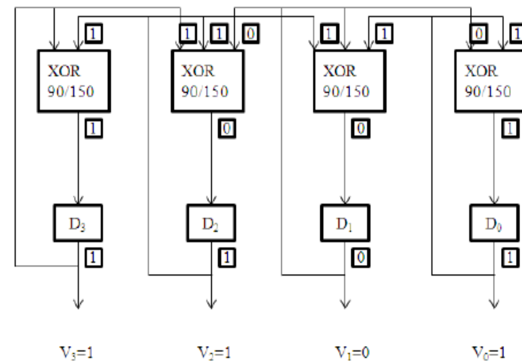

FIG 5: Cellular Automation

D. Low power Test Pattern Generator:
Here a Linear feedback shift register is used for generating test patterns with reduced switching activities. The LP-TPG consists of m bit counter, gray code generator, LP-LFSR, NOR gate structure and XOR gate.

The m bit counter is initialized with zeros, which generates 2^m test patterns. Counter and gray code generator are synchronized with common clock. When counter output is all zero pattern, NOR gate output is one. Only when the NOR gate output is one, the clock signal is applied to activate the LP-LFSR to generate the next seed. This seed and the output sequence from the gray code generator are exclusive OR to generate the final output. This effectively reduces the switching activities which results in low power.

For every 2^m clock cycles the seed value is changed and here no decoding logic is used. Also the selection of polynomial depends on number of faults to be covered which is not the case for other existing methods. So fault coverage is high and high randomness is introduced. The low power test pattern generator is shown in figure 6 in this circuit the power dissipation and power consumption will be less compare to other circuit.

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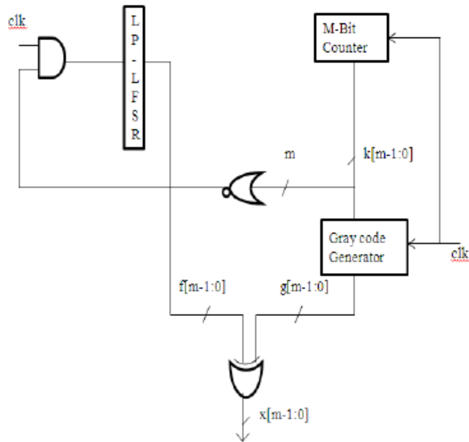

FIG 6: Low Power Test Pattern Generator

E. Vedic Multiplier

After implementing the Low Power Test Pattern Generator The 16-bit Vedic multiplier is used and the test pattern generating seed value is given to the 16 bit Vedic Multiplier

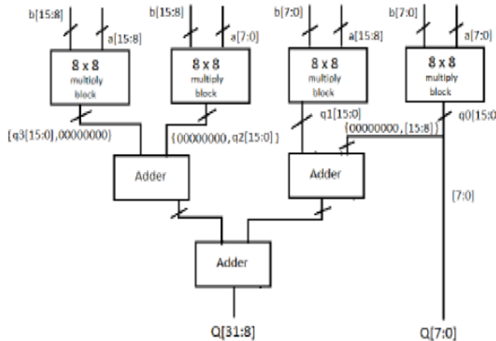

FIG 7: 16x16 Vedic Multiplier

II. LITERATURE SURVEY

For CMOS circuits and any type of IC's the circuit will be tested with the help of Built In Self Test, the power dissipation can be divided into static power dissipation and dynamic power dissipation. In general, static power consumption is from the leakage current and dynamic power consumption is from the switching transient current. For static power dissipation, the power consumption is proportional to the number of the used transistors. For dynamic power dissipation, the power consumption is obtained from the charging and discharging of load capacitance. For reduce the switching activity we can reduce the power dissipation, It is very important for testing the circuits to improve and to increase the fault coverage

[1] **Katti R.S , Ruan X.Y, and Khattri.H , "Multiple Output Low-Power Linear Feedback Shift Register Design," IEEE Trans. circuits & Systems .I,Vol.53, No.7,pp-1487- 1495,July 2006.**

In this paper they proposed a multiple output low power LFSR that produces the output of several clock cycles of a serial LFSR at once. This allows for a reduction in the power-supply voltage

[2] **Sybille Hellebrand , "Pattern Generation for a Deterministic BIST Scheme", ACM IEEE on CAD 95 (ICCAD- 95), San Jose, Nov 1995.**

In this they proposed pattern generation for a deterministic BIST scheme in which it targets test-per-scan architecture combining pseudo random and deterministic BIST. The amount of bits to be stored is reduced compared to others by 1-30%

[3] **Zorian.Y, " A Distributed BIST control Scheme for complex VLSI devices," Proc. VLSI test Symp,pp.4-s9,1993**

In this paper they proposed a distributed BIST control scheme for complex VLSI circuits in which a generic BIST scheduling process and BIST control architecture is presented. The control architecture provides an autonomous BIST activation and a diagnostic capability to identify failed blocks

[4] **Chakrabarty, et. al, "Deterministic Built-in Test Pattern Generation for High Performance Circuits Using Twisted-Ring Counters," IEEE Trans. of VLSI system, Vol. 8, No.5, pp. 633-636, Oct 2000.**

In this paper they proposed a deterministic Built-in Test Pattern Generation using Twisted-Ring Counter. It embeds a pre computed deterministic test set for the circuit under test (CUT) in a short test sequence produced by TRC. The patterns derived from the seeds are applied test-per-clock to the circuit under test. This is a combination of BIST with external slow testers

[5] **TEST PATTERN GENERATION USING PSEUDORANDOM BIST by GaneshBabu.J and Radhika.P**

In this paper they presented test-per-clock generation scheme, which can be utilized to efficiently generate weighted patterns without altering the structure of the adder. It does not impose any requirements about the design of the adder and operating speed is not affected. Benchmark net-lists demonstrate that the fault coverage of the proposed pattern generator is significantly higher compared to conventional pattern generation techniques.

[6] **Pseudorandom Testing – A Study of the Effect of the Generator** by **Peter fiser** and **Hana Kubatova**

In this paper they presented the influence of the pseudo-random pattern generator type on its fault detection capability. Both LFSRs and CA are studied, with either a random or a "special" seed. The distribution of weights on the individual PRPG outputs is shown for all cases, together with the fault coverage curves obtained by the PRPGs. We have shown that for a pseudorandom test-pattern generation phase a 1-tap LFSR is mostly a good choice, due to its satisfactory period length, fault coverage and minimal area overhead. in this paper, to help BIST designers properly choose the desired pseudo-random test lengths for these circuits. The effects of generator type are illustrated on a mixed-mode column-matching BIST synthesis. It directly influences the total complexity of the resulting BIST circuitry. The claims were confirmed experimentally on a BIST design for several ISCAS

benchmarks, but the conclusions made can be applied to any circuits.

[7] **Design and Implementation of 32bit Complex Multiplier using Vedic Algorithm** by **Ankush Nikam, Swati Salunke, Sweta Bhurse**.
The vedic method used here for complex multiplication is Urdhva Triyagbhyam‖ (vertically and Cross wise). Urdhva tiryakbhyam Sutra is the most efficient Sutra (Algorithm) that gives minimum delay for multiplication of small or large types of numbers.

[8] **Pipelined Vedic-Array Multiplier Architecture** by **Vaijyanath Kunchigi, Linganagouda Kulkarni** and **Subhash Kulkarni**.
In this paper the developed multiplier architecture is designed based on the Vedic and Array methods of multiplier architecture. The multiplier architecture is optimized in terms of multiplication and addition to achieve efficiency in terms of area, delay and power.

III. APPLICATION

1) The BIST is mainly used in the Automotive, Aviation and Integrating circuit manufacturing

2) The BIST is mainly used in the military which was the Minuteman was the first one of the major weapons systems to field a permanently installed

IV. CONCLUSION

In this paper a low power Test Pattern Generator has been incorporated in BIST developed for Vedic multiplier. The switching activities are reduced in the test pattern generation. Fault coverage is increased by the maximum number of clock cycles of the binary counter. The power consumption of different test pattern generation techniques has been found out and compared with the latest method. BIST is implemented for low power test pattern generator i.e. Vedic multiplier in the latest method. It is observed that the power consumption is reduced along with increased fault coverage when compared to other implementations.

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[9]. Pipelined Vedic-Array Multiplier Architecture by Vaijyanath Kunchigi, Linganagouda Kulkarni and Subhash Kulkarni. I.J. Image, Graphics and Signal Processing, 2014, 8, 58-64 Published Online May 2014 in MECS (http://www.mecs-press.org/) DOI: 10.5815/ijigsp.2014.06.08.